A 6 GHz Synthesized Local Oscillator For the W2PED 24 GHz Subharmonic Mixer

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INTRODUCTION

The author has presented a subharmonic mixer design for 24 GHz[1]. A Subharmonic mixer uses a lower frequency LO that is a sub-multiple of the normal LO input frequency. The unique feature of the mentioned mixer design is that it is based on a **x4** LO scheme, or requires an LO that's ¼ of that required for a standard type mixer, giving the advantage of simpler LO hardware. This is especially helpful in getting on a higher frequency band like 24 GHz. A synthesized 6 GHz LO is described here as a companion to the 24 GHz subharmonic mixer. The LO is locked to a 10 MHz reference; it uses the N5AC ApoLO-32 synthesizer followed by a frequency multiplier designed by the author.

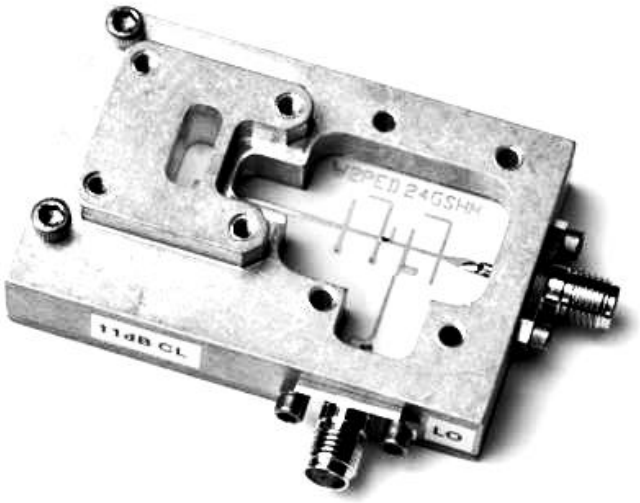

Figure 1 – W2PED 24 GHz Subharmonic Mixer

apolLO-32 SYNTHESIZER

Steve Hicks, N5AC has done a wonderful job designing a versatile and user-friendly high frequency synthesizer that operates in the 750-1300 MHz frequency range[2]. The synthesizer is an outgrowth of his USB controllable ApolLO-1 design and is intended as a replacement for the Down East Microwave MICRO-LO board. The board has over 50 pre-programmed frequencies that are user-selectable by choosing the appropriate several solder bridges. Among the internally programmed frequencies are several LO frequencies useful for the 24 GHz application for both 24048 MHz as well as 24192 MHz. The apolLO-32 board is shown below; the user-selectable pads may be seen at the right side of the board.

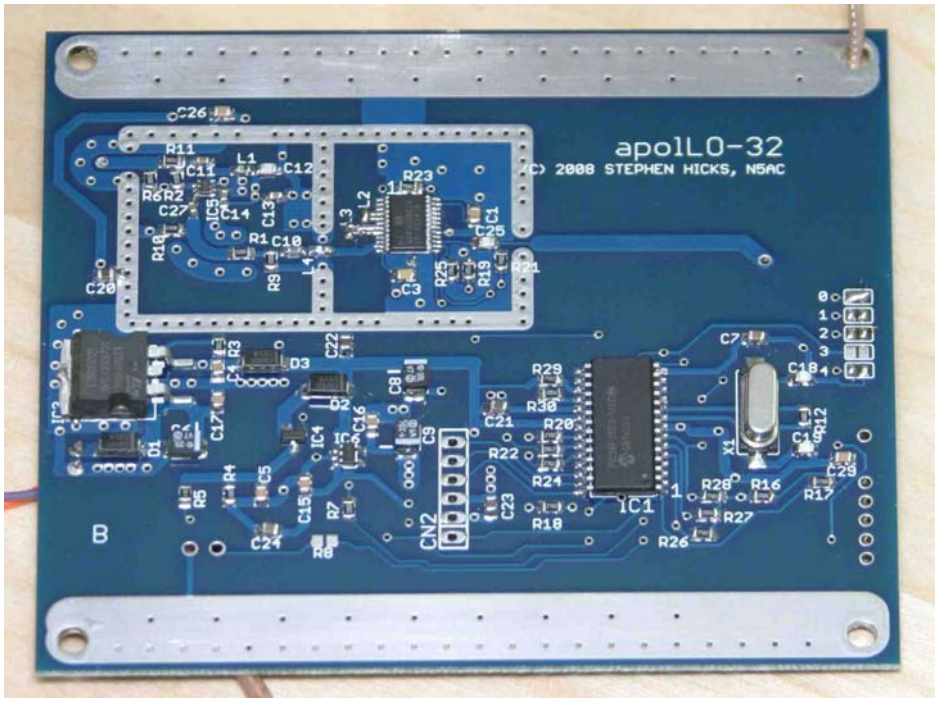

Figure 2 – N5AC apolLO-32 Synthesizer Board

More information regarding the apolLO-32 synthesizer may be found on the N5AC web site[3]. Boards may be purchased from the N5AC web site as well as through Down East Microwave[4].

LO BLOCK DIAGRAM

The overall block diagram of the local oscillator is quite simple. The apolLO-32 is locked to an external 10 MHz input. It's output is then multiplied x6 using a frequency multiplier board (described later). The LO output frequency is in the range of ~ 6 GHz as determined by the operating frequency and the chosen IF frequency. For clarity only round numbers are shown below.

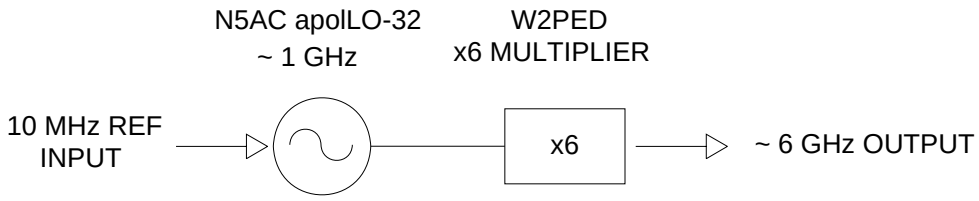

Figure 3 – 6 GHz Synthesizer Block Diagram

AVAILABLE FREQUENCY SCHEMES

A number of 24 GHz frequency schemes are available using the apolLO-32 internally programmed frequencies. The math is best illustrated by example; the case of a transverter using the subharmonic mixer operating at 24192 MHz with a 144 IF is illustrated below.

Subharmonic Mixer LO = (24192 –144) / 4 = 6012 MHz

Multiplier Input Frequency = 6012 / 6 = 1002 MHz

In this case, the mixer requires an LO of 6012 MHz. Since a x6 multiplier precedes the mixer LO input, the apolLO-32 needs to generate a frequency that's 1/6 of 6012 MHz, or 1002 MHz.

The currently available frequency schemes for operation at 24048 and 24192 MHz (low side injection) are shown below.

RF Freq	IF	LO Input
24048	144	996.000
24048	147	995.875
24048	432	984.000
24048	435	983.875

Figure 4 – 24048 MHz Frequency Schemes

RF Freq	IF	LO Input
24192	144	1002.000
24192	147	1001.875
24192	432	990.000
24192	435	989.875

Figure 5 – 24192 MHz Frequency Schemes

X6 FREQUENCY MULTIPLIER

Others have described MMIC frequency multipliers extensively in the amateur literature and Down East Microwave has effectively used them in a number of designs for the "No Tune" transverters. Anyone who would like to learn more about the use of MMIC amplifiers for frequency multipliers should get a copy of Jim Davey, WA8NLC's article published in the late 80's[5]. I just recently read (re-read) Jim's article and I probably could have saved myself a little time and effort had I done so sooner!

In this application with an output at 6 GHz, I considered using a MMIC as a x6 multiplier. Although the efficiency is poor with the higher order multiplication, in this application the filtering is fairly easy. Since the multiplier input frequency is at ~1 GHz, the nearest undesired multiples of 1 GHz will be at 5 GHz and 7 GHz (a bit easier than trying to filter out something 540 MHz away!). A 5-section microstrip edge-coupled bandpass filter looked to be a good choice to provide adequate filtering. A Mini-Circuits ERA-2 MMIC was chosen for the multiplier stage based on the fact that its gain response is fairly good past 6 GHz. The block diagram for the x6 multiplier chain is shown below.

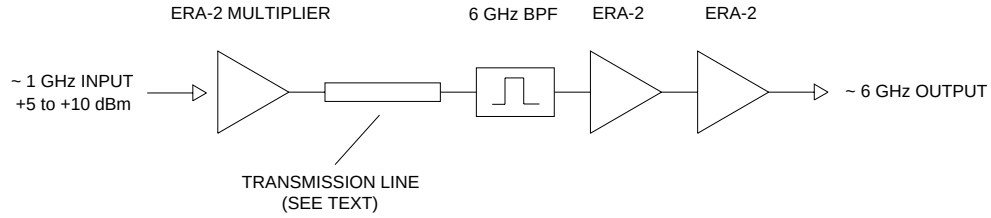

Figure 6 – x6 Multiplier Block Diagram

The board material I chose for this design is 30 mil thick Rogers 4350; I like this material as it's a good low loss high frequency board material but much lower cost than the teflon type boards. This board is considered a laminate substrate and looks and feels very similar to standard FR-4 / G-10 type board material except that it has an off-white appearance. Since this is essentially a "hard board," the PC board houses have an easier time processing this material, which also helps to keep the finished board costs more reasonable.

A 5-section edge coupled band pass filter was designed for the multiplier board. The measured filter response is shown below. Insertion loss is less than 3 dB and the return loss (not shown) is 15 dB. The filter needs to work over the 5900 to 6012 MHz bandwidth in order to cover all of the possible 24 GHz LO schemes. The measured response is centered at 6 GHz and has sufficient bandwidth to cover our needs for the multiplier application. The bandwidth was designed to be a little wider than necessary so that any etching tolerances at the board house wouldn't ruin our filter response. Note the undesired signals at 3, 4, 5, 7, and 8 GHz should be attenuated by many dB!

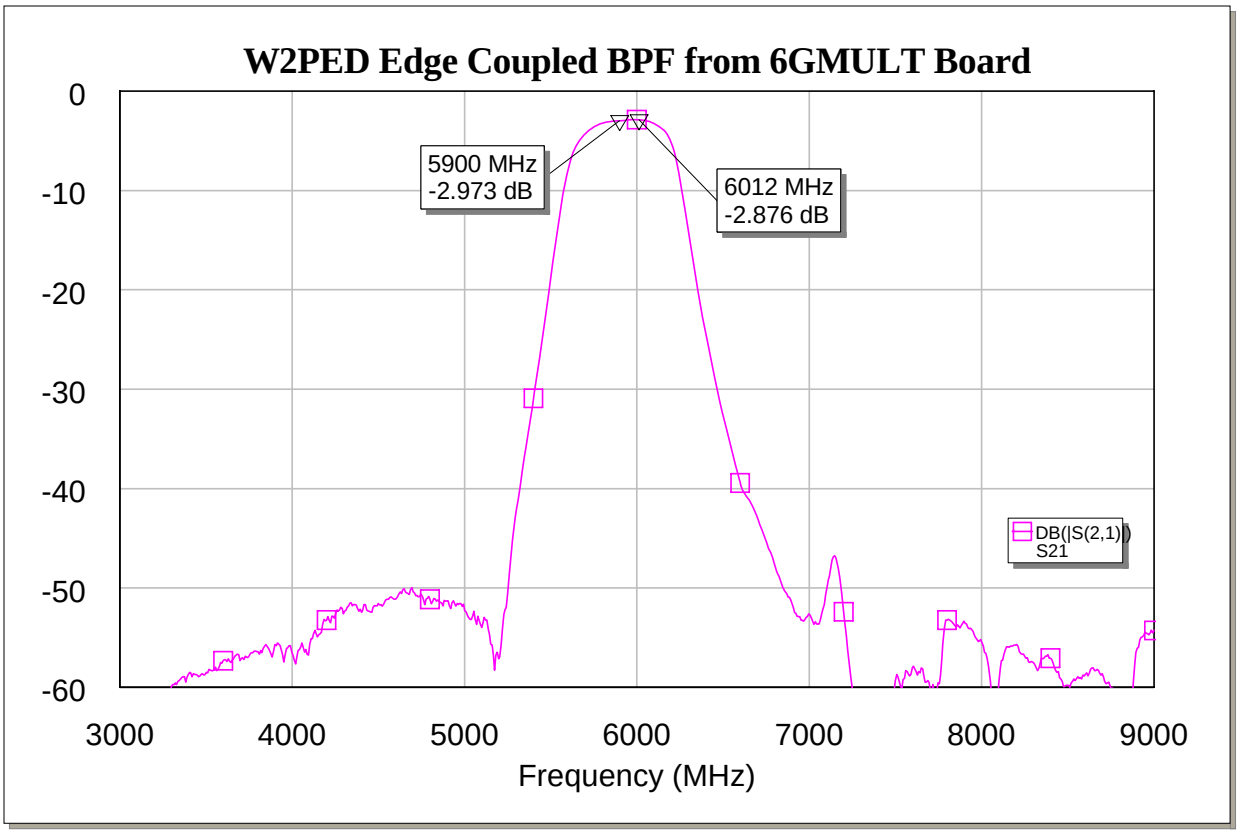

Figure 7 – Measured Response of Edge Coupled BPF

It was found that the multiplier stage works best with an input signal of ~ +5 to +10 dBm. Increasing the RF input level past +10 dBm results in greatly increased spurious signals and no increase in output energy at 6 GHz. In fact, if the RF input is continued to increase, the output level actually *decreases*. The multiplier chain (like most multipliers) is drive level sensitive.

INITIAL PERFORMANCE

Several prototype multipliers were built using the above filter design and the ERA-2 MMICs. Initial results were pretty good – with +5 to +10 dBm input, the high frequency output was +8 to +10 dBm. The MMICs were biased at their recommended bias point of 40 mA; no attempt was made to further optimize the circuit performance with DC biasing. The spectrum analyzer however, showed that there were undesired spurs present at ~250 MHz away from each side of the desired output signal. The spurs were in the neighborhood of -35 dBc. I tried a number of things to improve the spur levels including input drive level, additional tuning (shunt C at various points) and various external filters at the multiplier input. I was able to tune a number of boards to have spurs on the order of -40 dBc. While this was probably "good enough for amateur work" I really wasn't happy with the spurious performance and the amount of tuning time required on each board.

IMPROVEMENTS FOR SPURIOUS

During a conversation with Steve Kostro, Steve reminded me that the 1989 article by Jim Davey indicated that the multipliers "work best" with a transmission line added between the multiplier circuit and the band pass filter. I couldn't find my copy of the mentioned article, but started to think about this a bit. Around the same time I also saw an old HP App note that included a transmission line after a Step Recovery Diode multiplier, but made no mention as to why[6]. After mulling over the situation, I realized that the fundamental energy at the MMIC multiplier output was likely the culprit to the undesired spurious levels; the fundamental level at the output of the device is probably *at least* 10 dB above the x2 and x3 energy and many more dB above the desired x6 energy. The BPF is reflective out of band and looks like a short or open circuit anywhere outside of the 6 GHz pass band; all of the fundamental energy was being reflected back to the device output and causing who-knows-what additional distortion inside the multiplier device. The mathematical possibilities of these products were almost mind-boggling!

I next built up a prototype MMIC multiplier by itself, along with a separate BPF, both with SMA connectors. When various cable lengths were inserted ahead of the BPF, it looked like a quarter wavelength transmission line at the fundamental frequency greatly improved the spurious output. It seems that the fundamental energy is undergoing a 90˚ phase shift, reflecting off the BPF, undergoing a second 90˚ phase shift, and arriving back at the device output 180˚ out of phase. This is illustrated below.

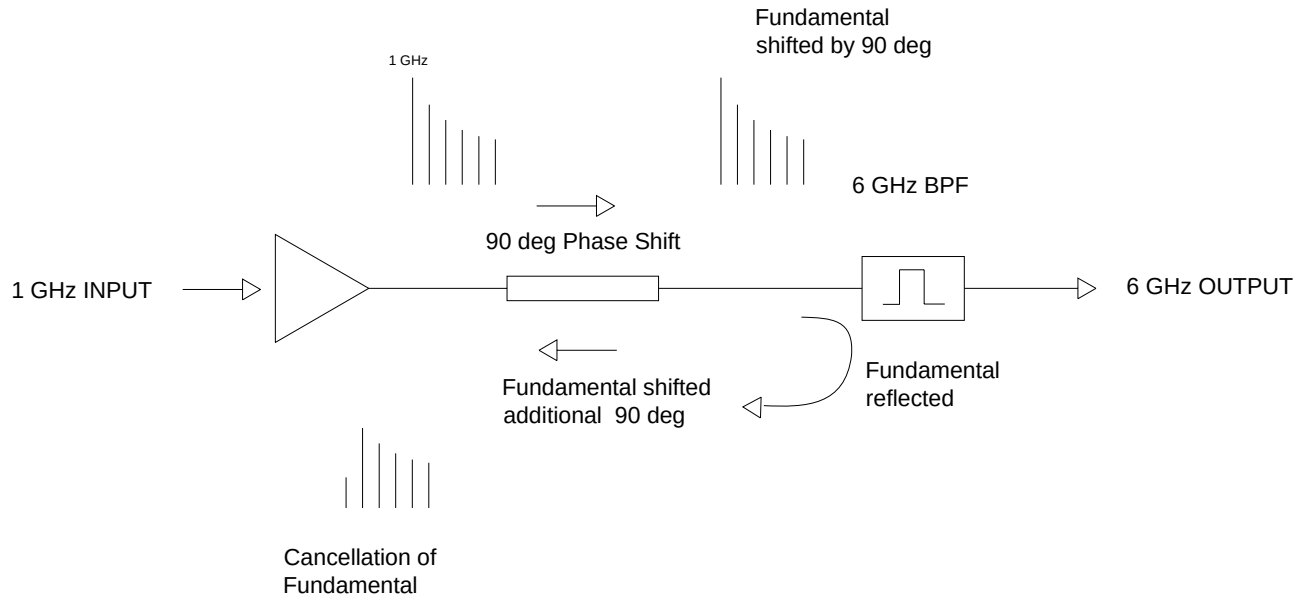

Figure 8 – Cancellation of Fundamental Energy

Since the amplitude and phase relationships are likely not 100% perfect, the cancellation is limited but the net effect is that the close-in spurious signals are all but eliminated and the next closest spurious energy at 5 GHz is now down 50-55 dB from the desired. The experiment showed a 15-20 dB improvement over the original lineup.

Once I proved out the relationship with coaxial lines, I repeated the experiment using a microstrip line. The final board layout incorporated this length and also allowed provisions to shorten the line length by a small amount. In practice, I found that a small capacitor (2-3 pF) placed to ground along this line provided a helpful phase adjustment. In addition to improving the spurious signals, the desired signal actually *increased* by several dB over the case where no additional transmission line was used. This is apparently due to the reflected energy improving the efficiency of the multiplier circuit. Jim's article and an HP App note[7] discuss this phenomenon. Perhaps the greatest benefit from all this is that the revised multiplier boards are now *much* easier to test and tune and are very repeatable.

A spectrum analyzer plot of the final multiplier circuit is shown below. The RF input was at 1002 MHz at +10 dBm. The 6012 MHz output measures -12 dBm. The worst-case spurious signal at 4 GHz is now -45 dBc. All others are improved to better than -50 dBc… more than sufficient for our mixer local oscillator!

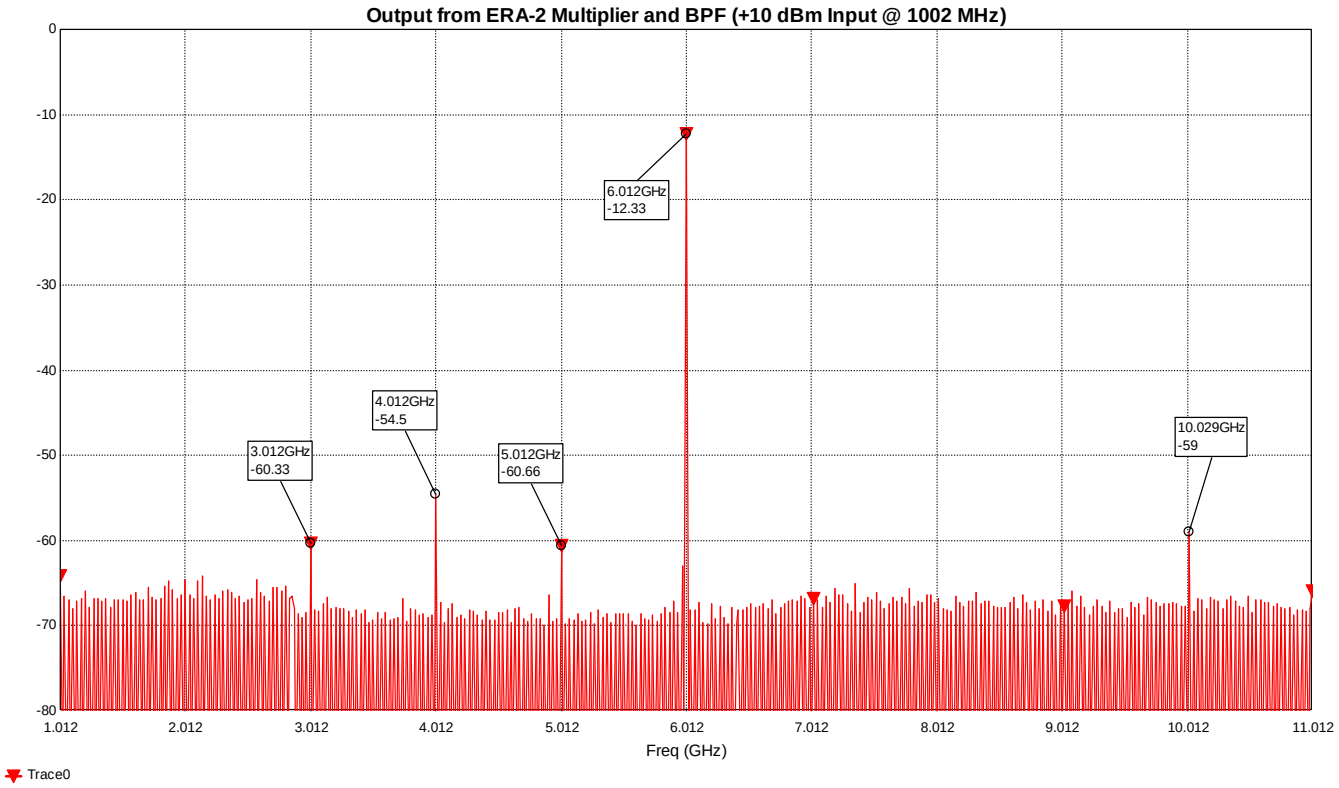

Figure 9 – Output of MMIC Multiplier with Transmission Line and BPF

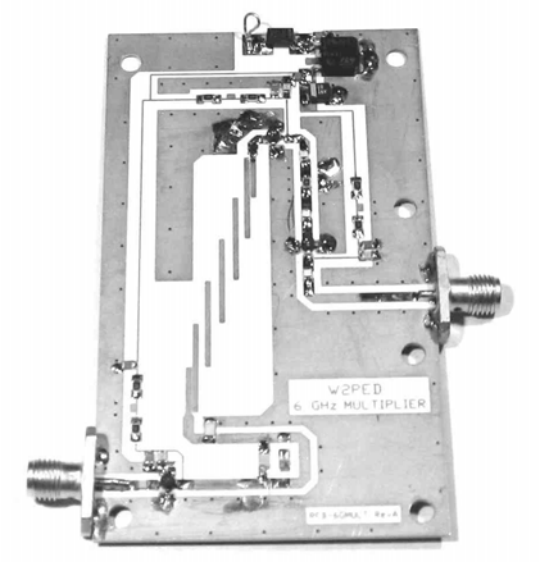

Figure 10 – Assembled 6GMULT Board

The assembled multiplier is shown above. The input is at the lower left, and the output at the upper right. The MMIC multiplier stage can be seen at the lower left adjacent to the SMA input connector. A serpentine microstrip line forms the quarter wavelength line prior to the band pass filter input. Additional gain stages are seen following the BPF.

The last plot shows the complete multiplier chain as seen on a spectrum analyzer. The center signal is at 6012 MHz; power output is +9 dBm with +10 dBm input at 1002 MHz. Some low level spurs can be seen at 4, 5, 7, and 8 GHz; the worst offender is at 4 GHz and is ~55 dB down from the desired. The spurious response has been improved even further due to the shunt C “phase tweek” capacitor. Note that the close-in spurs seen on the plot are from the signal generator being used. While the plot below illustrates performance at an output frequency of 6012 MHz, similar results are obtained with the other frequency schemes. The assembled 6 GHz LO using the apolLO-32 synthesizer gives nearly identical results to those shown.

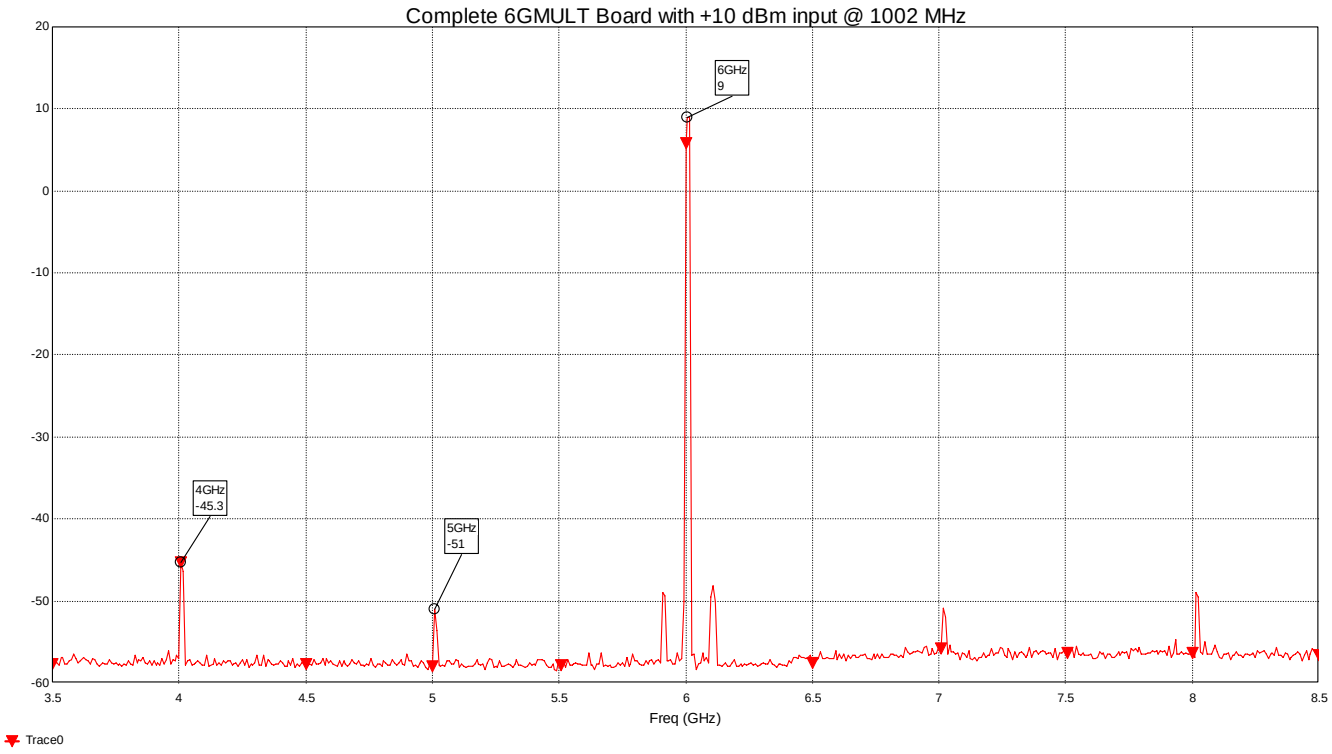

Figure 11 – Spectrum Analyzer Plot of Assembled 6GMULT Board

The assembled 6 GHz LO is shown below. The boards are packaged in one of the housings available from DEMI. A connector for the 10 MHz reference input is on the rear panel, and RF Output and lock indication is provided on the front panel.

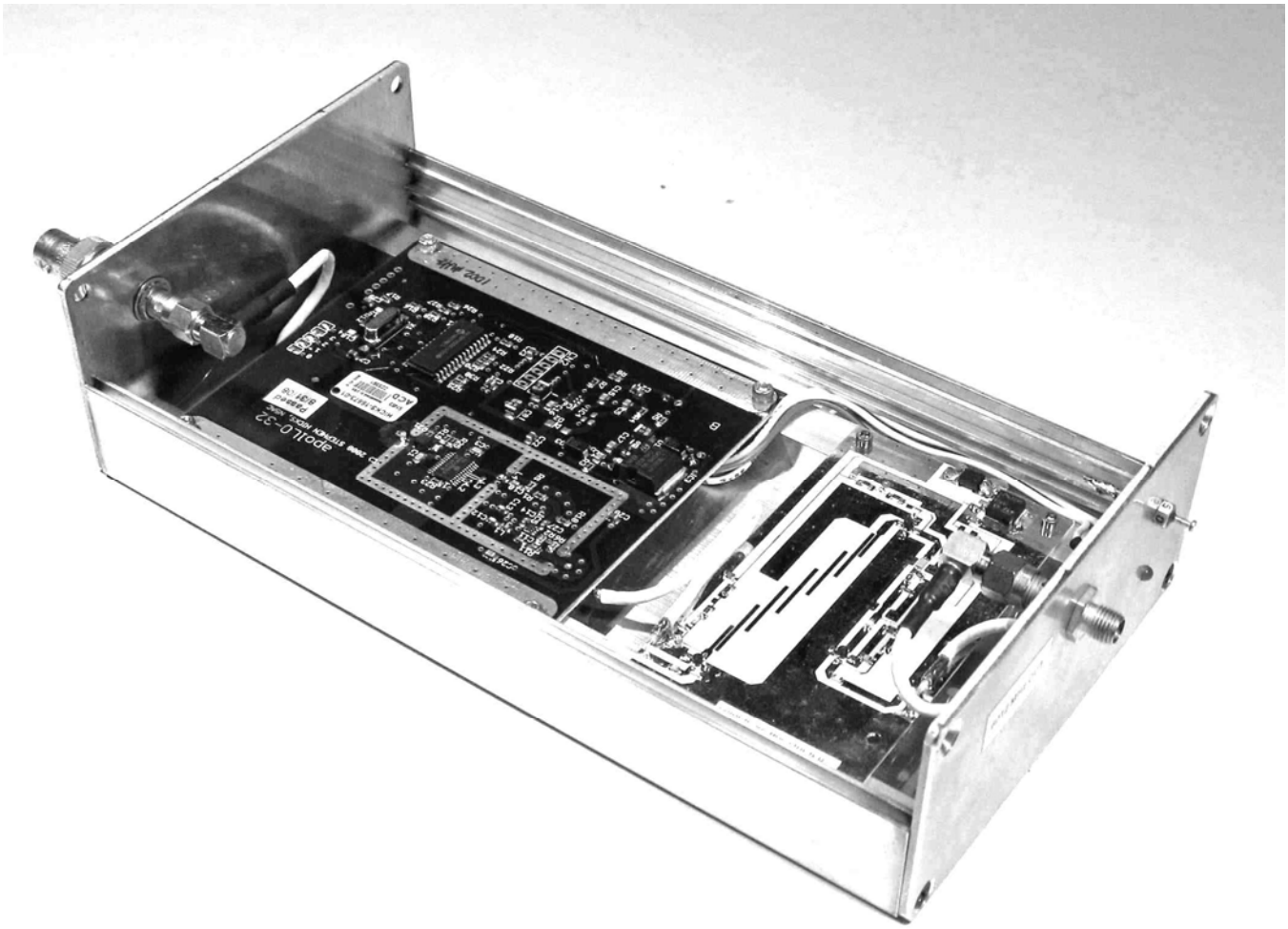

Figure 12 – Interior View of Assembled 6 GHz LO

CONCLUSION

A synthesized 6 GHz LO has been designed as a companion to the W2PED 24 GHz subharmonic mixer. The author is providing complete LO assemblies as well as multiplier boards for those who may be interested in getting on the 24 GHz band.

73, Paul Drexler w2ped

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[1] P. Drexler, W2PED, "A x4 Subharmonic Mixer for 24 GHz," Proceedings of Microwave Update 2008
[2] S. Hicks, N5AC, "A USB Programmable High Stability LO for Microwave Transverters," Proceedings of the 2008 Southeastern VHF Conference.
[3] www.n5ac.com
[4] www.downeastmicrowave.com
[5] Jim Davey, WA8NLC, "Frequency Multipliers using Silicon MMICs," Proceedings of Microwave Update 1989
[6] "Step Recovery Diode Multipliers," HP App Note AN920
[7] "Comb Generator Simplifies Multiplier Design," HP App Note AN983